



WMH-5

Packaging and Integration Solutions at Terahertz Frequencies

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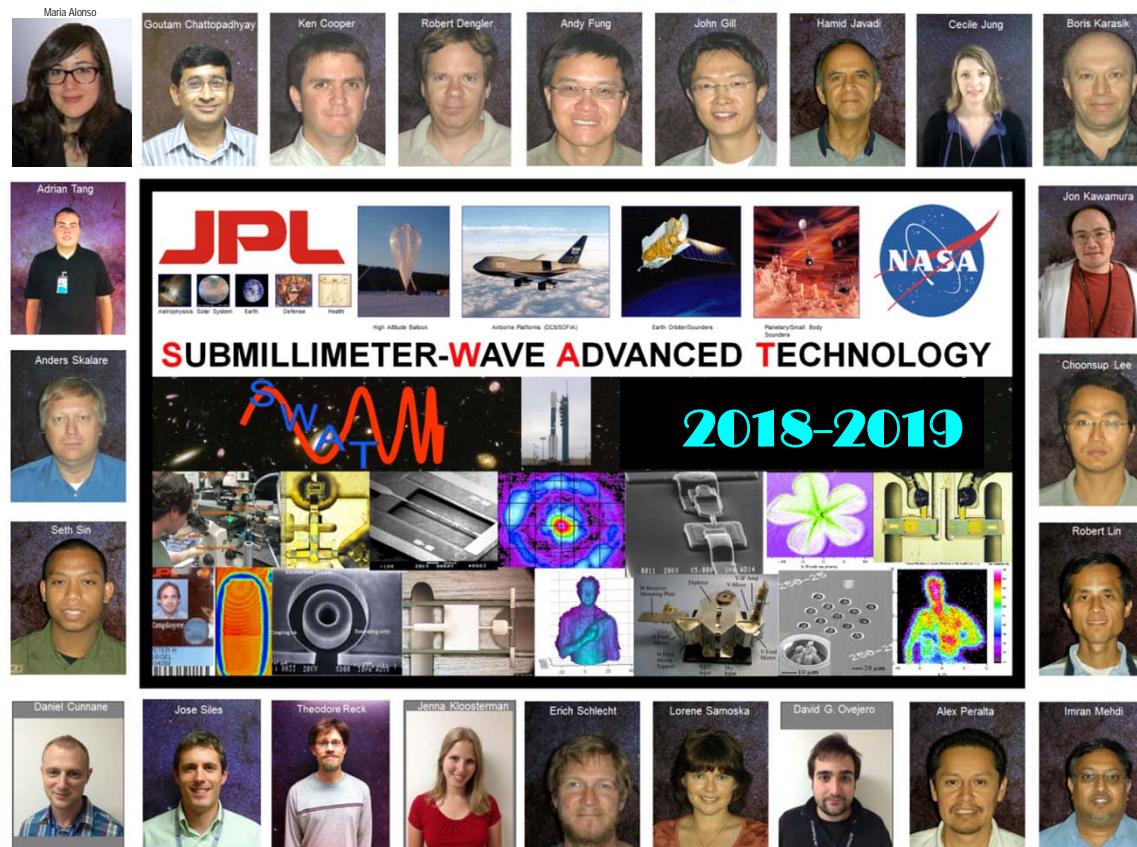


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WMH-Recent Advancement and Trends in 3D heterogeneous integration for mmW 5G and Terahertz



Acknowledgement

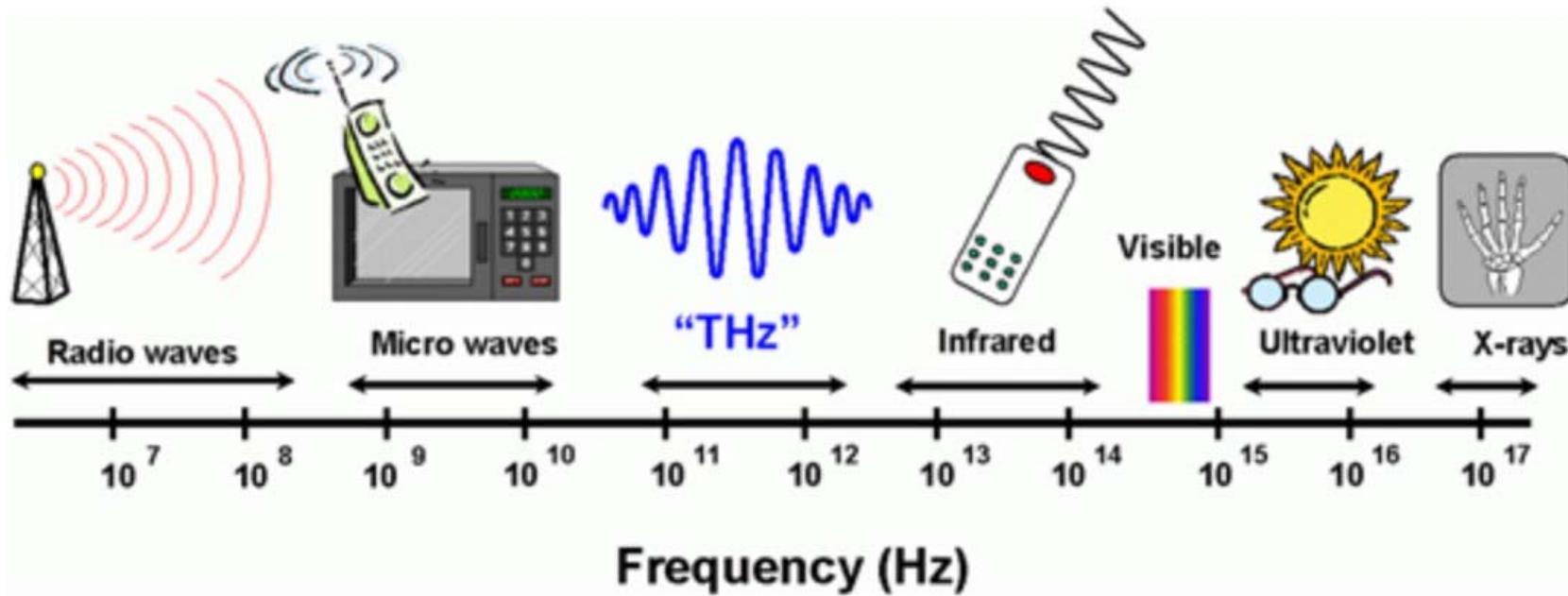


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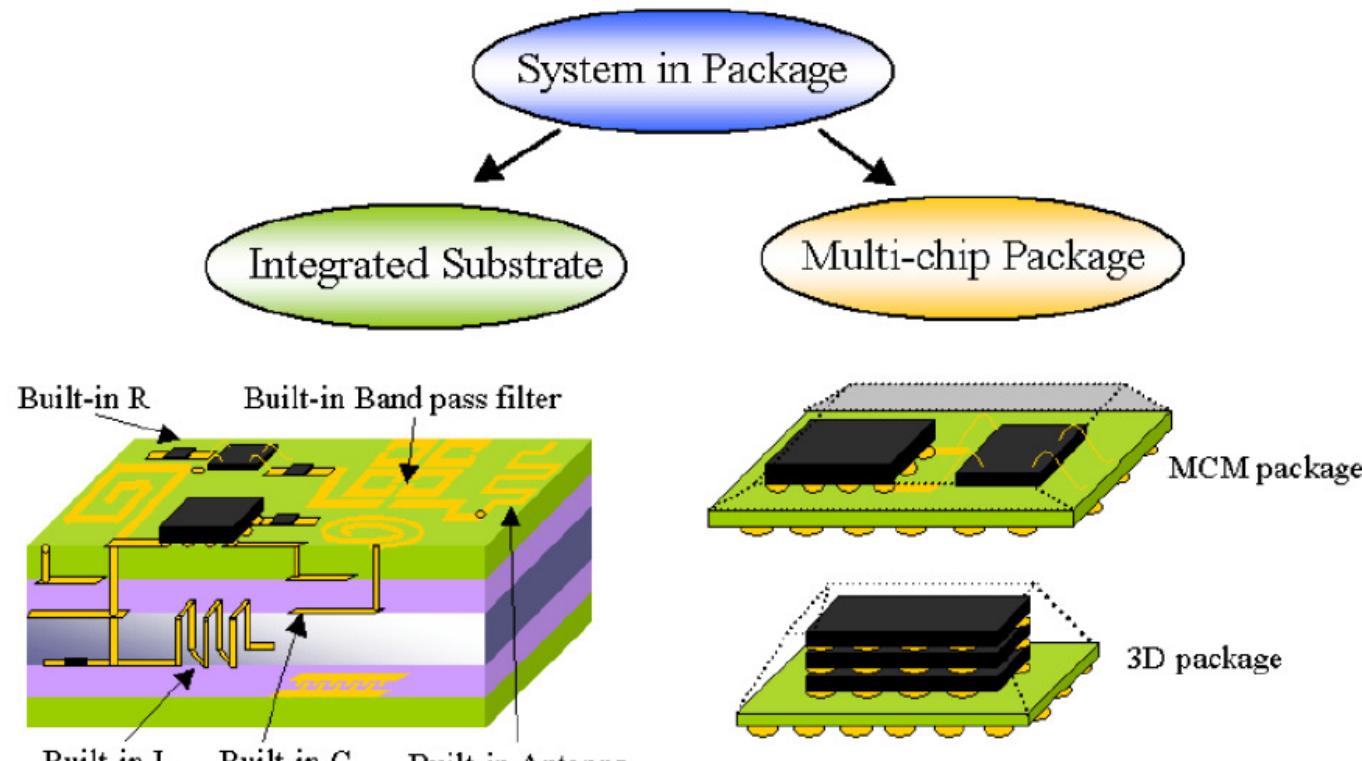
Terahertz (Submillimeter) Waves



Loosely defined: $1 \text{ mm} > \lambda > 100 \mu\text{m}$ ($300 \text{ GHz} < \nu < 3 \text{ THz}$)

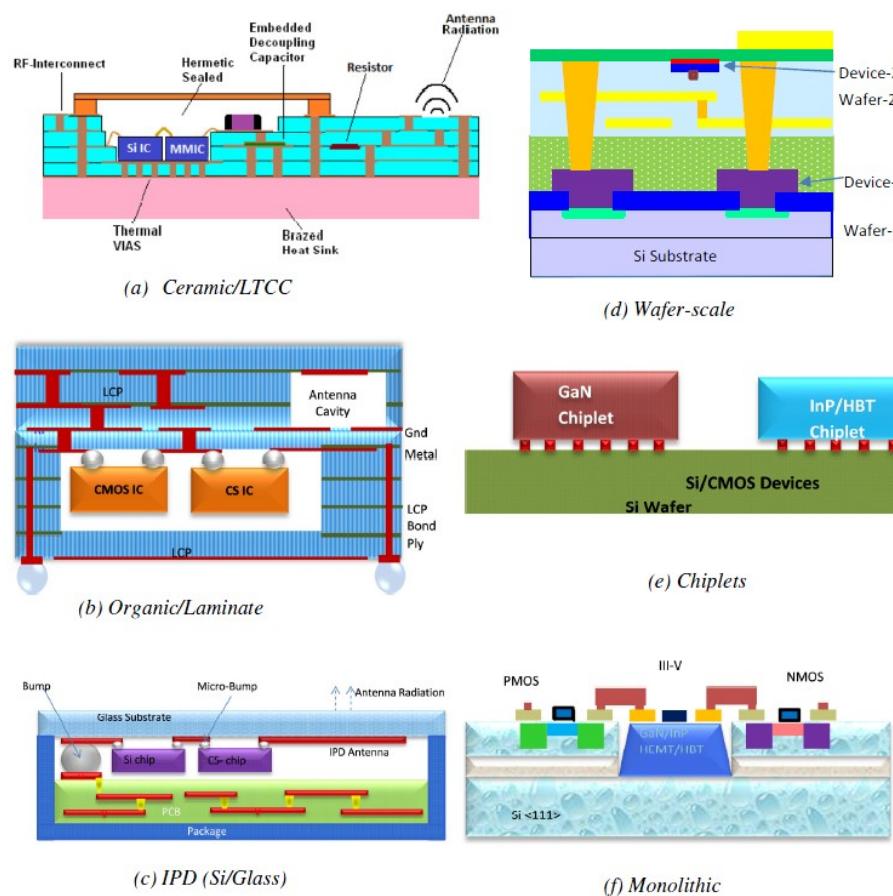
Most of the radiation in the Universe is emitted at submillimeter-wavelengths, peaking at 3 THz.

Packaging at Millimeter-Waves



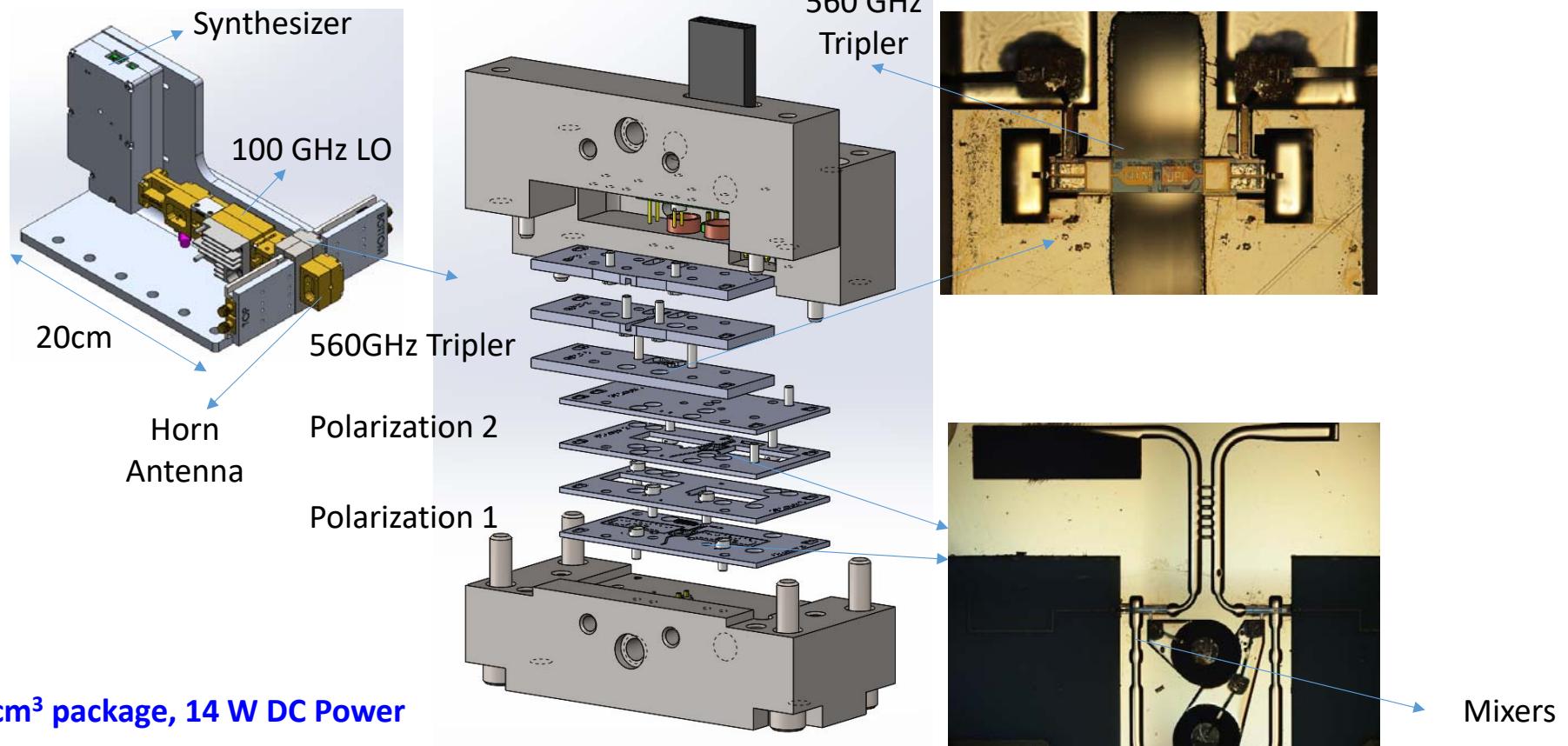
Different System-on-Package (SOP) Technologies

Packaging at Millimeter-Waves



Multi-layer heterogeneous integration: Ceramic LTCC based, Organic Laminate based, Si/Glass based, Wafer-scale, Chiplets based. (Ref: K. Samanta)

Packaging at Submillimeter-Waves

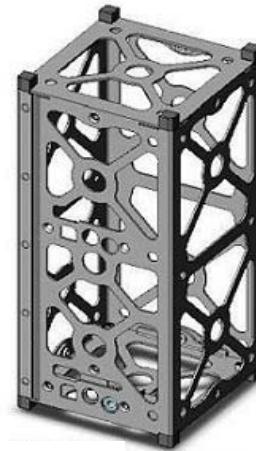
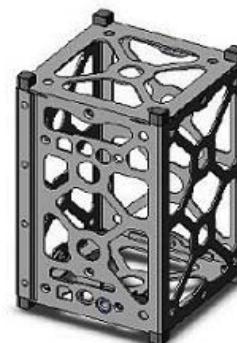


CubeSat and SmallSat Platforms

What are CubeSats?

Cubes of 10 cm x 10 cm x 10 cm: 1 U

1U

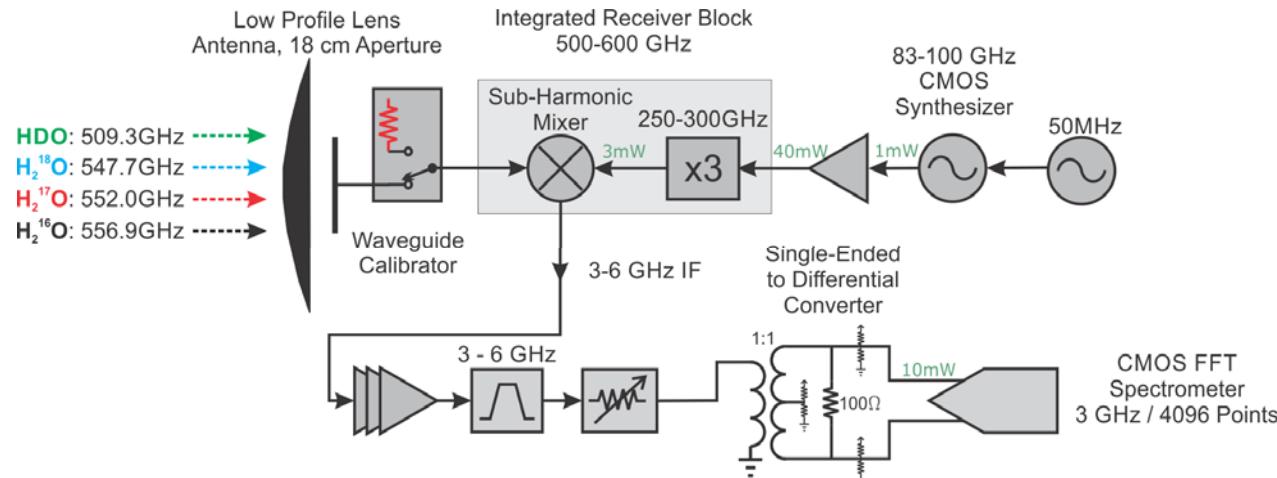


3U

A shoe-box size satellite: includes navigation, communications, antennas, solar panels, and instruments, all on the CubeSat!



Typical Terahertz Systems



- High-resolution room temperature heterodyne spectrometer 500-600 GHz band
- Low-profile ~18 cm diameter aperture antenna and feed
- Low-power CMOS based W-band synthesizer
- GaAs Schottky diode based subharmonic mixers and frequency multipliers
- CMOS based 3 GHz bandwidth, 4096 channels, low-power FFT spectrometer
- The target mass and power for the instrument is less than 2 kg and <5 W.

Silicon Micromachining

Silicon Micromachining

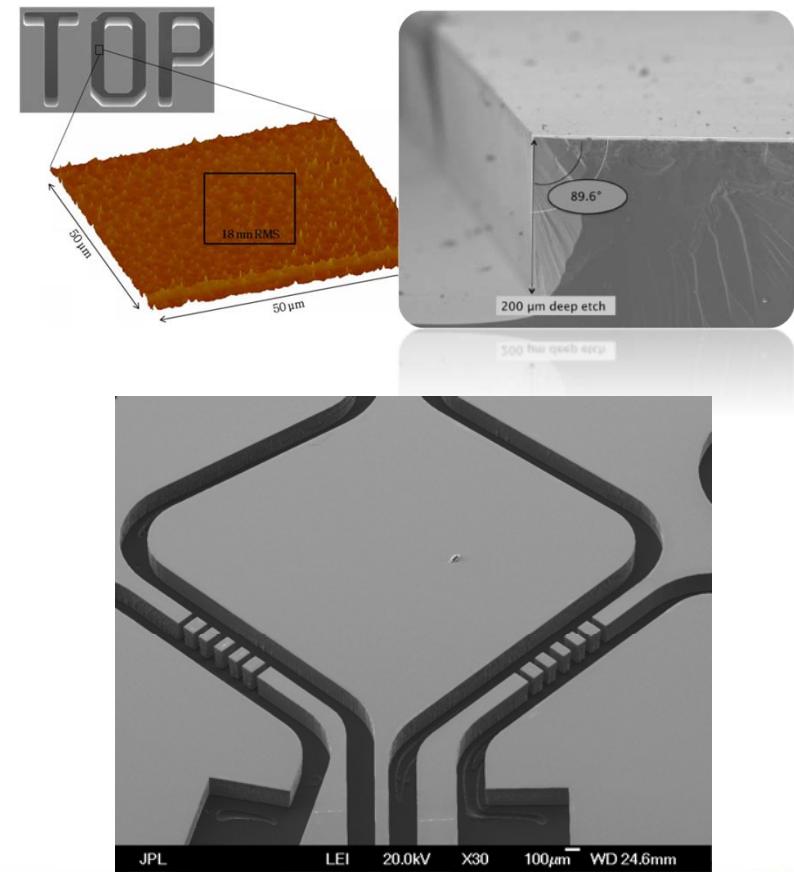
- Etch silicon wafer with plasma using a photolithographic pattern

Advantages:

- Potential for lower cost because of batch-processed device fabrication, yielding better uniformity too.
- Lithographically precise feature definitions
- Integration of bias & IF lines on silicon itself. Future potential for integrated CMOS silicon devices.
- Potential for higher density 2D transceiver arrays.

Disadvantages:

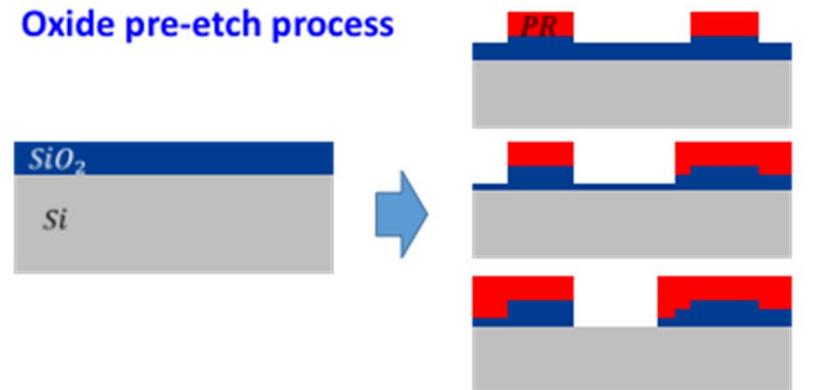
- Immature technology: need for process development:
Not anymore!
- Challenge of wafer alignment.



Deep Reactive Ion Etching

- Use of an optimized **Bosch** process to etch the silicon: alternative exposures of SF_6 and C_4F_8 plasmas.

Oxide pre-etch process



- Use of SiO_2 as hard mask (selectivity 150:1) to etch Si
- Use of photoresist to do the SiO_2 patterning
- Etching of the differential pattern to ensure precise control
- Etching using Inductive Couple Plasma (ICP) process

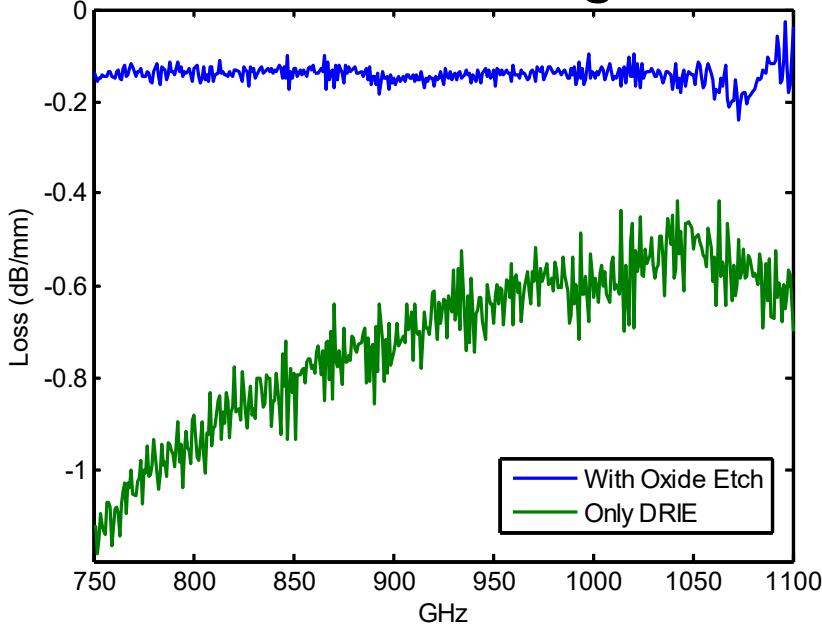


DRIE process

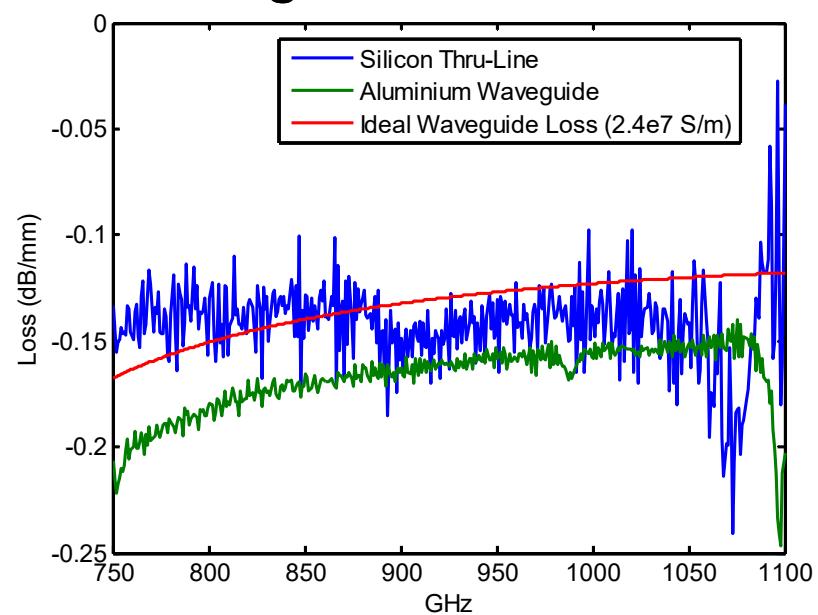
- DRIE process to etch the silicon, with oxide as the sole mask
- No photoresist

Deep Reactive Ion Etching

Effect of Etch Roughness



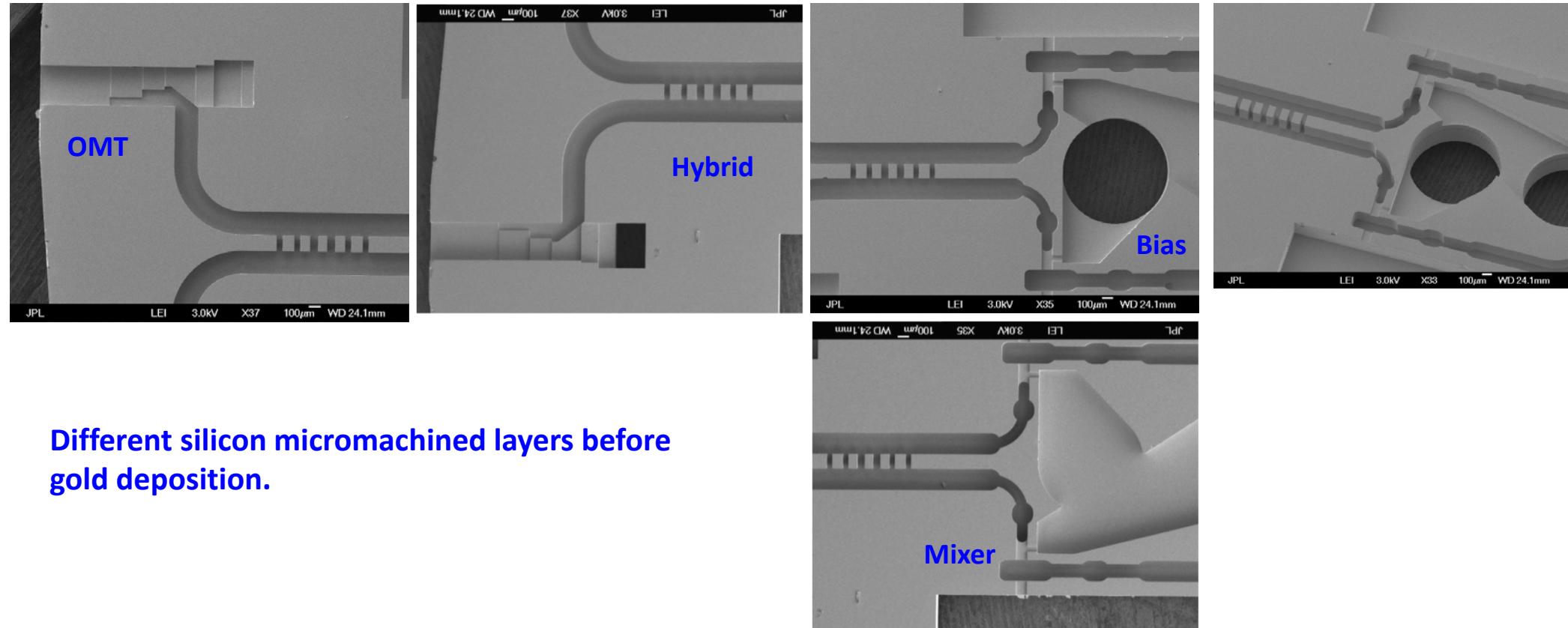
Waveguide Loss: Thru Lines



- Roughness from the DRIE process results in a roughness of 335nm—too high for these frequencies
- 2um of thermal oxide grown over wafer (1um into and 1um added to wafer)
- Oxide removed with wet etching
- Process smooth rough features since oxide will penetrate peaks more than valleys**



DRIE Components



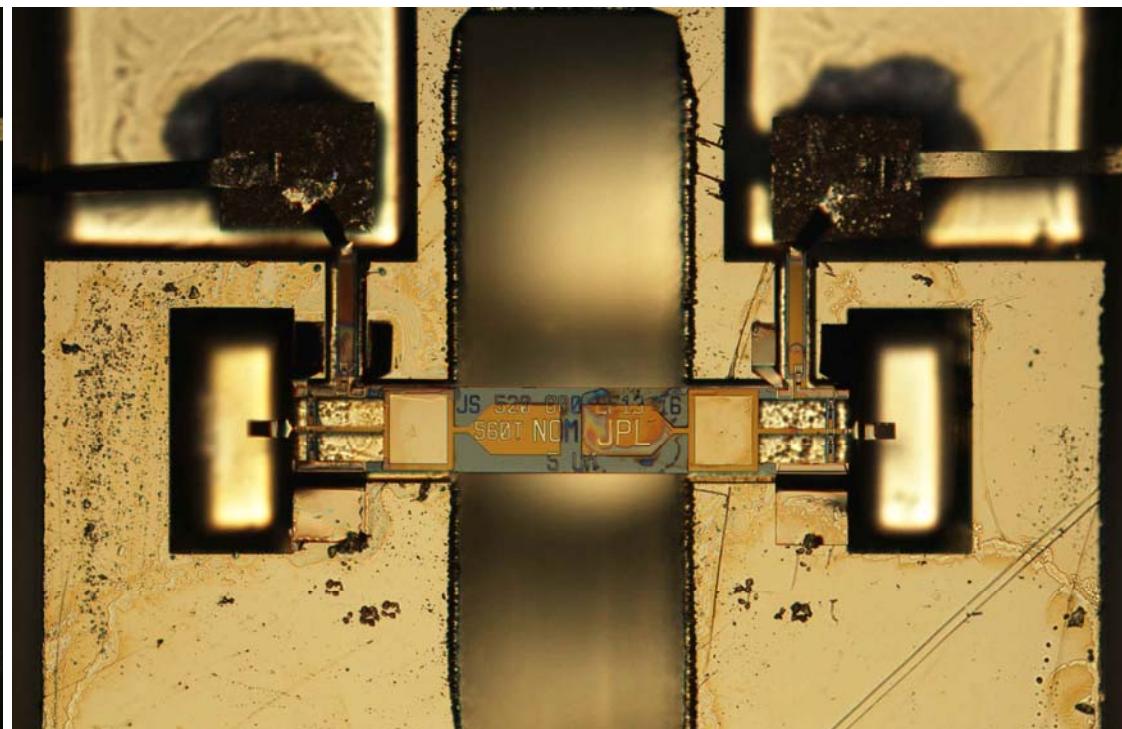
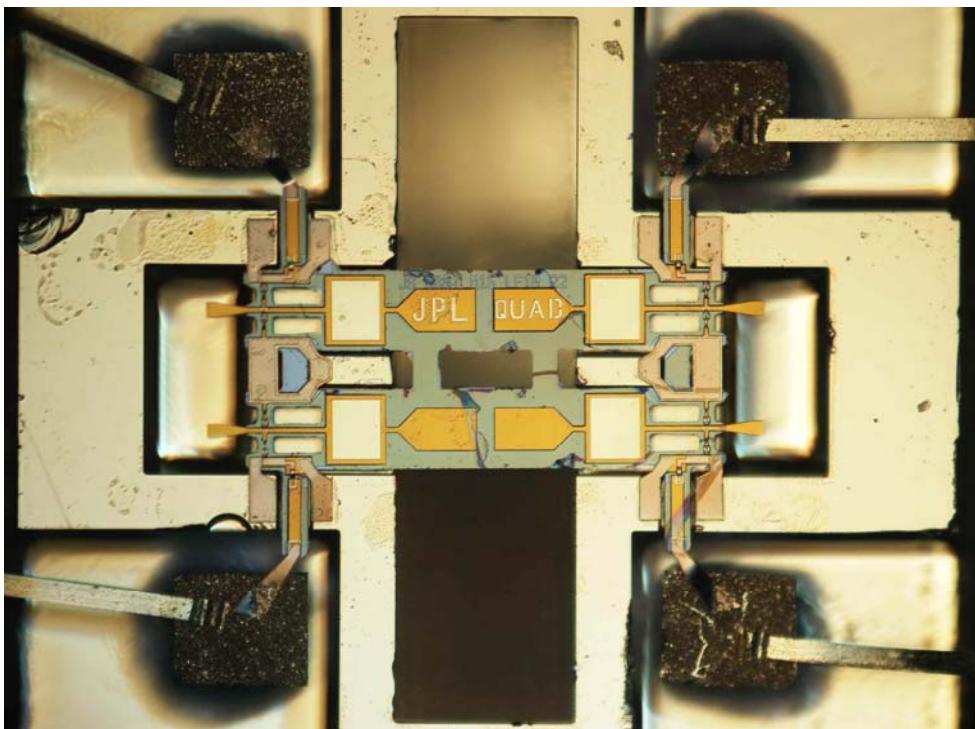
Different silicon micromachined layers before gold deposition.



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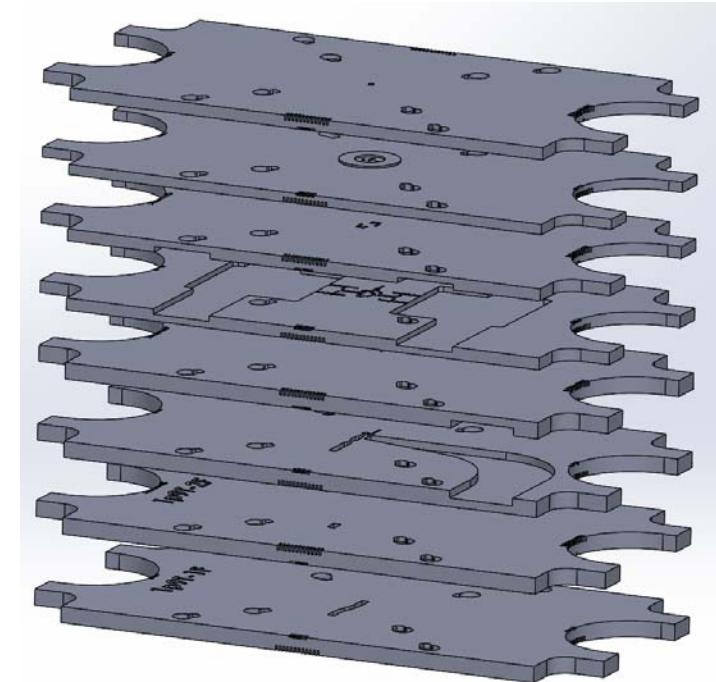
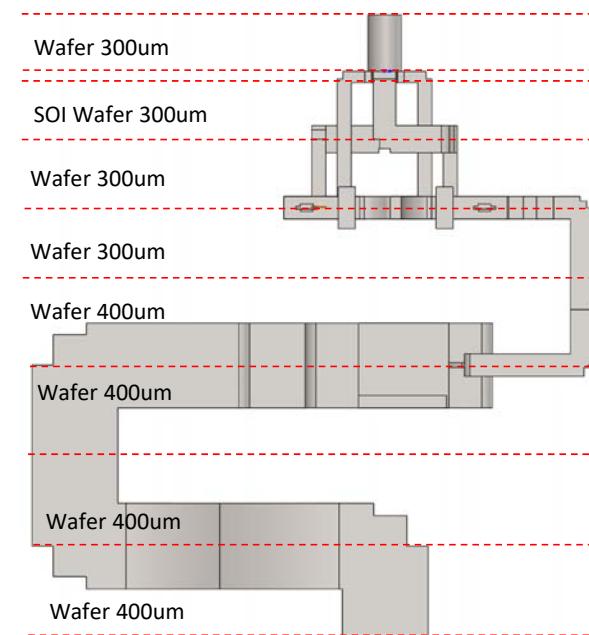
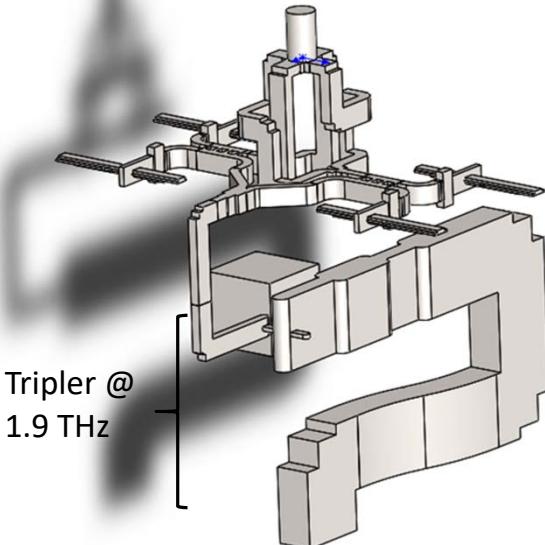
Integration of Active Devices



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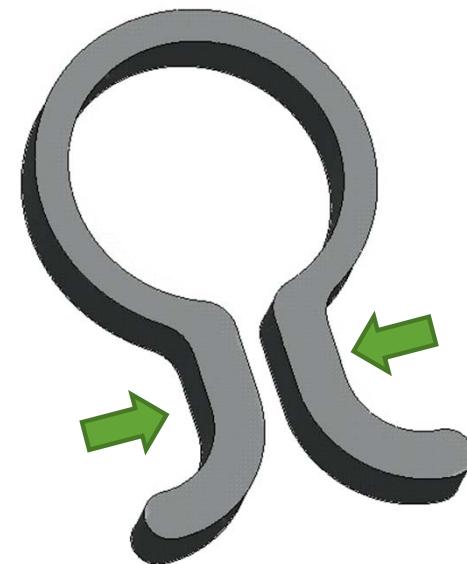
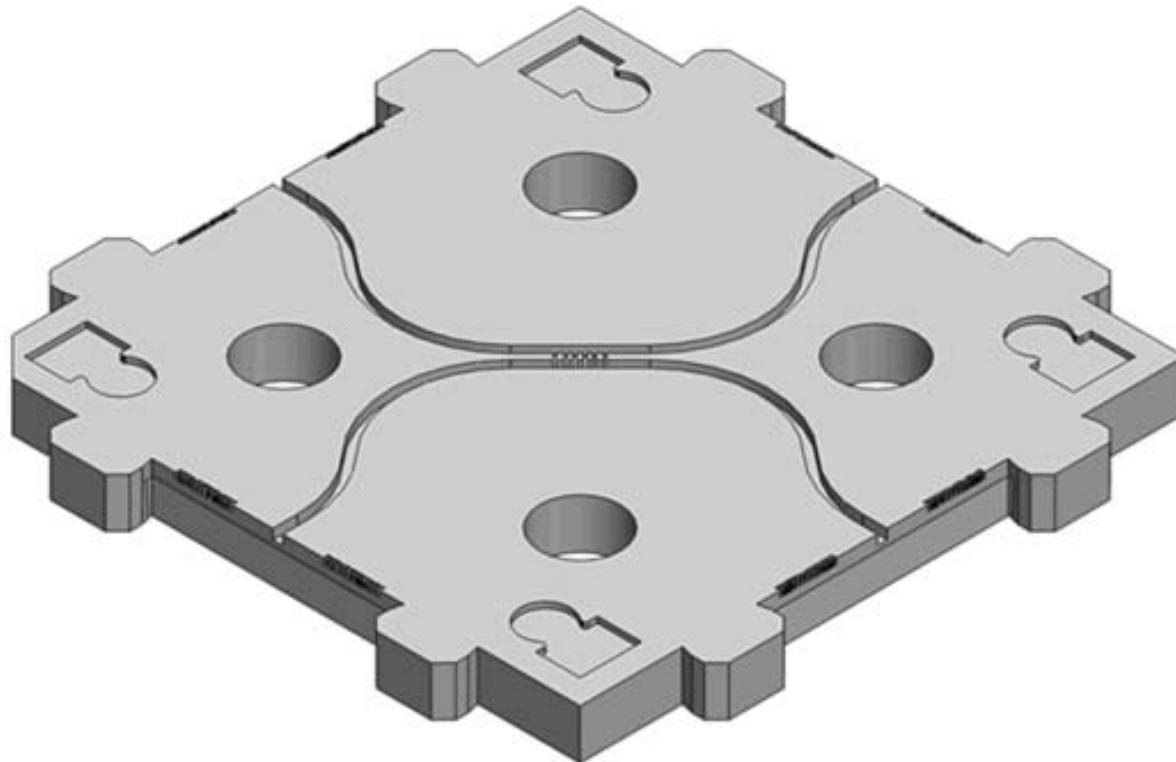
Vertical Integration

- Waveguide structures are fabricated on silicon wafers and **coated with gold**, stacked vertically





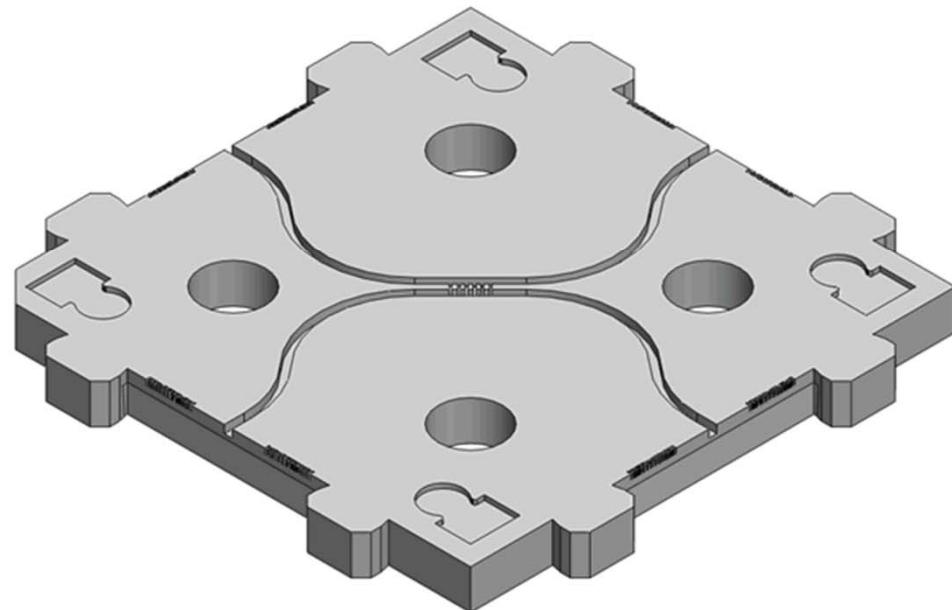
Alignment of Silicon Wafers



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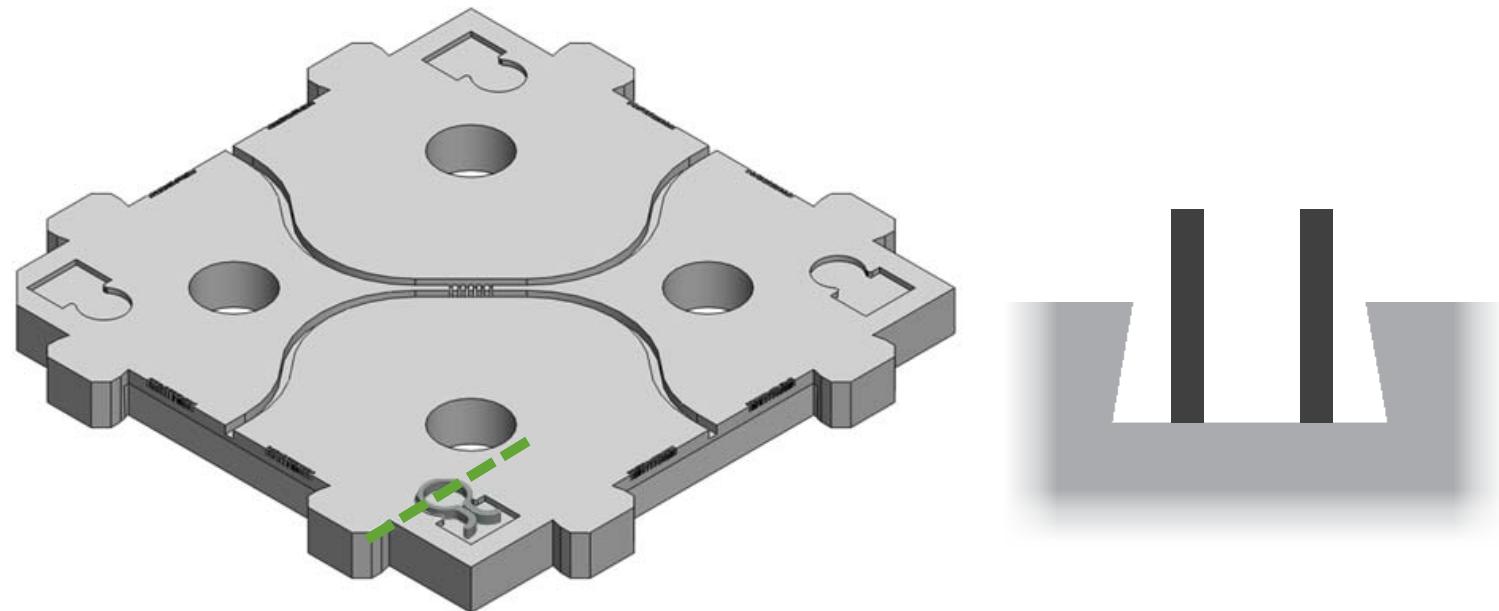
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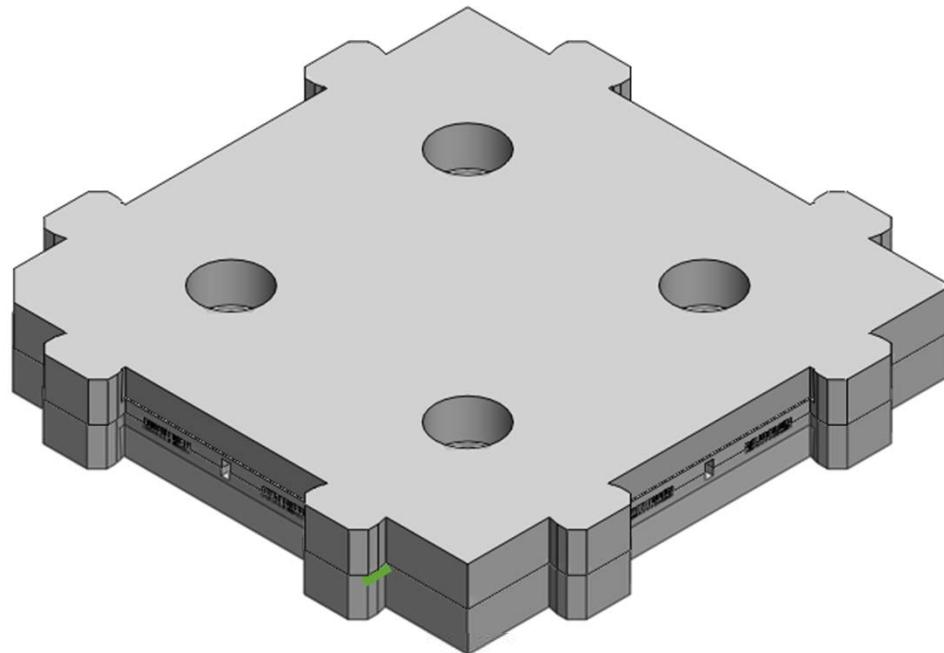
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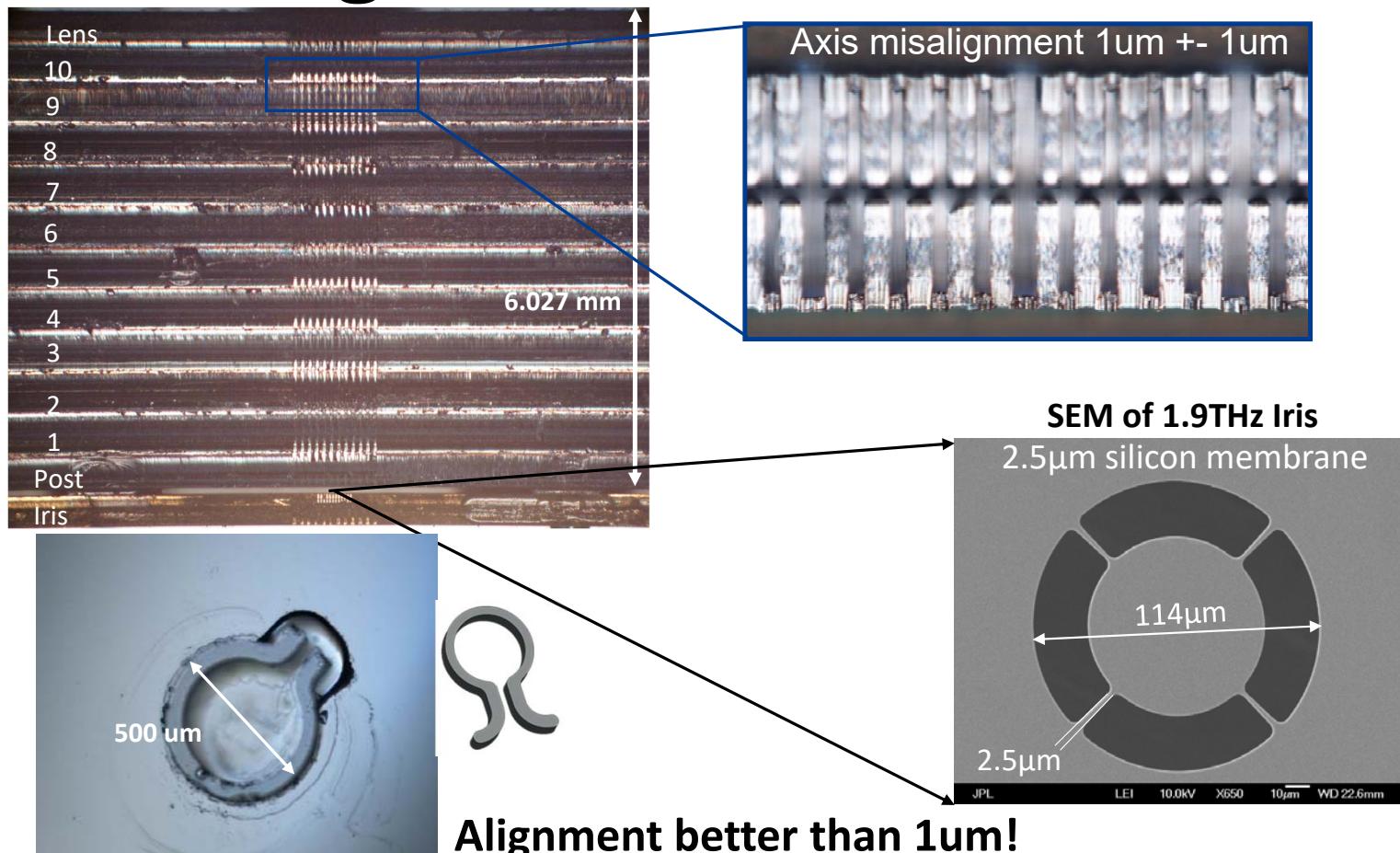


Alignment of Silicon Wafers

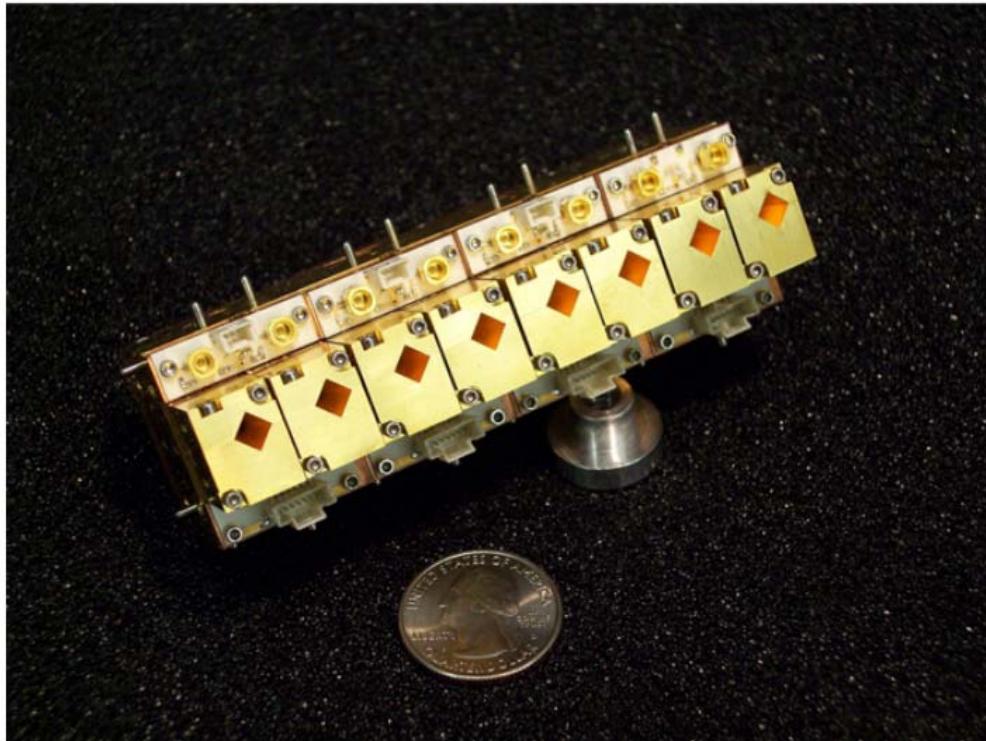


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Alignment of Silicon Wafers



Integrated System



handgun,
outside pocket of
leather jacket



handgun,
inside pocket of
leather jacket



8-Pixel Fully Functional 340 GHz Imaging Radar System.



Summary



- Packaging is a challenge at millimeter-wavelengths
- It gets much harder at terahertz frequencies.
- Silicon micromachined waveguide based packaging seems to be a practical solution.



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